

| | Type | Hits | Search Text | DBs | Time Stamp | Comments | Error Definition | Errors |
|----|------|------|---|----------------------------------|---------------------|----------|------------------|--------|
| 47 | BRS | 9 | (Nishizawa-Hirotaka.in. Ishihara-Haruji.in. Shiraishi-Atsushi.in. Kanemoto-Kouichi.in. Yukawa-Yousuke.in.) and card and @pd>20030725 | USPAT; US-PGPUB; EPO; JPO | 2004/03/05 09:59 | | | 0 |
| 48 | BRS | 478 | (361/822.ccls. 361/763.ccls. 361/764.ccls. 439/60.ccls. 902/25.ccls. 902/26.ccls. 361/42.ccls. 340/7.32.ccls. 439/180.ccls. 439/630.ccls. 174/255.ccls. 257/679.ccls. 361/737.ccls. 235/441.ccls. 235/492.ccls.) and @pd>20030725 | USPAT; US-PGPUB | 2004/03/05 10:08 | | | 0 |
| 49 | BRS | 30 | ((ic chip smart circuit memory) adj1 card\$1) same ((resin epox\$3 encapsul\$4 mould\$3) near5 (terminal\$1 contact\$3 pin\$1) near5 (cover\$3 cas\$3 body shell hous\$3)) | USPAT; US-PGPUB | 2004/03/05 15:11 | | | 0 |
| 50 | BRS | 30 | ((ic chip smart circuit memory) adj1 card\$1) same ((resin epox\$3 encapsul\$4 mould\$3) near5 (terminal\$1 contact\$3 pin\$1) near5 (cover\$3 cas\$3 body shell hous\$3)) | EPO; JPO; DERWENT; IBM_TDB | 2004/03/05 14:50 | | | 0 |
| 51 | BRS | 302 | ((ic chip smart circuit memory) adj1 card\$1) same (resin epox\$3 encapsul\$4 mould\$3) same (terminal\$1 contact\$3 pin\$1) same (cover\$3 cas\$3 body shell hous\$3) | USPAT; US-PGPUB | 2004/03/05 16:45 | | | 0 |
| 52 | BRS | 272 | ((ic chip smart circuit memory) adj1 card\$1) same (resin epox\$3 encapsul\$4 mould\$3) same (terminal\$1 contact\$3 pin\$1) same (cover\$3 cas\$3 body shell hous\$3)) not (((ic chip smart circuit memory) adj1 card\$1) same ((resin epox\$3 encapsul\$4 mould\$3) near5 (terminal\$1 contact\$3 pin\$1) near5 (cover\$3 cas\$3 body shell hous\$3))) | USPAT; US-PGPUB | 2004/03/05 15:14 | | | 0 |

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|----|------|------|--|----------------------------------|---------------------|----------|------------------|--------|
| 53 | BRS | 264 | ((ic chip smart circuit memory) adj1 card\$1) same (resin epox\$3 encapsul\$4 mould\$3) same (terminal\$1 contact\$3 pin\$1) same (cover\$3 cas\$3 body shell hous\$3) | EPO; JPO; DERWENT; IBM_TDB | 2004/03/05 16:46 | | | 0 |
| 54 | BRS | 234 | ((ic chip smart circuit memory) adj1 card\$1) same (resin epox\$3 encapsul\$4 mould\$3) same (terminal\$1 contact\$3 pin\$1) same (cover\$3 cas\$3 body shell hous\$3)) not ((ic chip smart circuit memory) adj1 card\$1) same ((resin epox\$3 encapsul\$4 mould\$3) near5 (terminal\$1 contact\$3 pin\$1) near5 (cover\$3 cas\$3 body shell hous\$3))) | EPO; JPO; DERWENT; IBM_TDB | 2004/03/05 16:46 | | | 0 |
| 55 | BRS | 24 | ((ic chip smart circuit memory) adj1 card\$1) same (parallel near5 serial near5 mode\$1) | USPAT; US-PGPUB | 2004/03/05 17:37 | | | 0 |
| 56 | BRS | 21 | ((ic chip smart circuit memory) adj1 card\$1) same (parallel near5 serial near5 (terminal\$1 contact\$1)) | USPAT; US-PGPUB | 2004/03/05 17:56 | | | 0 |
| 57 | BRS | 1 | ((ic chip smart circuit memory) adj1 card\$1) same (parallel near5 serial near5 (terminal\$1 contact\$1)) | EPO; JPO; DERWENT; IBM_TDB | 2004/03/05 17:44 | | | 0 |
| 58 | BRS | 1092 | ((ic chip smart circuit memory) adj1 card\$1) same (usb (universal adj serial adj bus)) | USPAT; US-PGPUB | 2004/03/05 17:47 | | | 0 |
| 59 | BRS | 294 | ((ic chip smart) adj1 card\$1) same (usb (universal adj serial adj bus)) | USPAT; US-PGPUB | 2004/03/05 17:48 | | | 0 |
| 60 | BRS | 24 | ((ic chip smart) adj1 card\$1) same ((usb (universal adj serial adj bus)) near5 (terminal\$1 pin\$1 contact\$1)) | USPAT; US-PGPUB | 2004/03/05 17:52 | | | 0 |
| 61 | BRS | 8 | ((ic chip smart) adj1 card\$1) same ((usb (universal adj serial adj bus)) near5 (terminal\$1 pin\$1 contact\$1)) | EPO; JPO; DERWENT; IBM_TDB | 2004/03/05 17:52 | | | 0 |

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|----|------|------|--|----------------------------------|---------------------|----------|------------------|--------|
| 62 | BRS | 64 | ((ic chip smart circuit memory) adj1 card\$1) same ((communication near5 mode\$1) near5 (terminal\$1 pin\$1 contact\$1)) | USPAT; US-PGPUB | 2004/03/05 18:08 | | | 0 |
| 63 | BRS | 18 | ((ic chip smart circuit memory) adj1 card\$1) same ((communication near5 mode\$1) near5 (terminal\$1 pin\$1 contact\$1)) | EPO; JPO; DERWENT; IBM_TDB | 2004/03/05 18:08 | | | 0 |